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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,924	IKARASHI, YASUHIRO	
	Examiner	Art Unit	
	michael b. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-21,23-26 and 28-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-21,23-26 and 28-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 43 is objected to because of the following informalities: It is clear that applicant meant "the plurality" for "the plutality". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-12, 14, 20, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh 6,737,927 (Hsieh) in view of Segawa et al. 6,342,818 (Segawa).

Figure 1(a) and the relevant text of Hsich discloses a signal generator and associated method of generating a signal. The invention of Hisich includes a voltage controlled oscillation circuit means (vco) 14 that generates a voltage controlled signal output, a control input terminal means V_{cntrl} for inputting an control voltage for determining a frequency of an oscillation signal at the output of the voltage controlled oscillator and a frequency divider circuit means 16 for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit. Figure 1(a) and the relevant text of Hsich also discloses a frequency divided signal output terminal means CLKO for outputting a frequency divided signal output from the frequency divider circuit and a buffer amplifier 15 which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the frequency divider circuit wherein the buffer amplifier 15 has a balanced input and an unbalanced output and thus converts the balanced oscillation signal to an unbalanced output oscillation signal. Note that the loop filter would form part of the "first control means" as recited by claims like claim 21.

Hsich is silent on calling the signal generated at the output of the frequency divider a "wide frequency range", however, since no specific definition of "wide frequency range" appears in the original disclosure, Hsich is seen as meeting the limitation. This is just giving the broadest reasonable interpretation to the claims (See MPEP 2111). However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the component values such that a "wide frequency range" is obtained, since it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105, USPQ 233.

Hsich recites that the frequency division ratio is a divide by "two" circuit. Note that "two" is a whole number and as such Hsich is seen as meeting the limitations of claims like claim 14. Hsich is silent on calling this "controlling a frequency division ratio", but there must be some circuitry within the frequency divider 16 of Hsich that controls the frequency division ratio to "two" and as such Hsich is seen as meeting the limitations of claims like claim 26. Hsich is also silent on selecting the frequency division ratio to be such that the frequency divided signal output has a frequency that is equal to or lower than the frequency of the oscillation signal. Adjustable frequency dividers are conventionally known in the art. Also selecting the division ratio is a result effective variable that controls the output frequency of the frequency divider. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the frequency divider 16 adjustable so as to allow for output frequencies of different values including output frequencies that is equal or lower than the frequency of the oscillation signal, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954). Furthermore, the selection of the amount of frequency division is seen as part of the workable or optimum range for Hsich as this selection is merely the selection of a result effective variable. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the frequency division ratio to be such that a output frequency of equal to or lower than the frequency of the oscillation signal is obtained, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105, USPQ 233.

Hsich is silent on the integration of at least the vco and the frequency divider. It is well known to integrate the vco and the frequency divider into a single integrated circuit (ic). Note column 17 around line 55 of Segawa. The well-known advantage to forming an ic is that it forms a more compact, and typically more reliable structure as compared to a circuit formed from just discrete components.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed at least the vco and the frequency divider of Hsich as an ic so as to make for a more compact and more reliable structure over that of a circuit formed of discrete components as taught by Segawa.

Hsich is silent on whether the loop filter that provide the control voltage to the vco is external or internal. However, it is common knowledge in the art that forming the filter element outside, i.e. external the integrated circuit or inside, i.e. internal the integrated circuit that includes a vco and a frequency

divider are art recognized equivalent structures. See column 17 around line 60 of Segawa. Therefore, because these two filter means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute an external filter for an internal filter and a internal filter for a external filter in a vco based circuit such as that of Hsich. Thus when the external filter is utilized in Hsich this provides an external control voltage to the vco of Hsich.

With respect to claims like claim 6, Hsieh is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that has the frequency control controlled by a FET functioning as a voltage controlled variable capacitor. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Hsieh with one at employs a FET functioning as a voltage controlled variable capacitor because as the Hsieh reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that has a FET functioning as a voltage controlled variable capacitor used to control the frequency of the vco.

With respect to claims like claim 7, Hsieh is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that is formed utilizing CMOS technology. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Hsieh with one that is formed utilizing CMOS technology because as the Hsieh reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that is formed utilizing CMOS technology.

With respect to claims like claim 11, Hsieh is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Hsieh with one that that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor wherein the frequency of oscillation of the vco is controlled by the external voltage applied to the varactor diode as the Hsieh reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor wherein the frequency of oscillation of the vco is controlled by the external voltage applied to the varactor diode.

With respect to claims like claim 10, the combination made obvious above is silent on placing the ic on a circuit board with the control voltage terminal and the frequency division signal output terminals

are provided on the end faces or on the underside of the circuit board. It is well-known to place ic's on circuit boards and provide the contacts on the underside of the circuit board so as to provide for a package that allows the mounting of the ic and the connection of the ic to other circuits. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the ic made obvious above on a circuit board with underside contacts so as to allow for the ic to be mounted and connected with other circuits in a device or system as is conventionally known in the art to do so.

Claims 13, 15, 21, 24, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh 6,737,927 (Hsieh) in view of Segawa et al. 6,342,818 (Segawa) as applied to claims 1, 5-12,14, 20, 26, 28 above, and further in view of Berquist et al. 6,542,044 (Berquist).

Hsieh are both silent on the use of controlling the frequency divider 16 of Hsieh by an externally applied switching signal. Hsieh is also silent on the construction of the frequency divider 16. Hsich is also silent on controlling a frequency division ratio of the frequency divider by a "second control means".

Berquist discloses that a frequency divider can be composed of elements 155 and 158 to divide the frequency at the output of the vco (See the paragraph bridging columns 4 and 5). This frequency divider works on an externally applied switching signal 263. Note that digital signal is considered a switching signal because of the "zero" and "one" values of the signal, i.e. it is "on" or "off". This allows for the value of the frequency divider to be changed and controlled in a fractional manner that allows for finer frequency control (See column 4, around line 54).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the frequency divider 16 of Hsieh in the combination made obvious above with a frequency divider such as Berquist so as to allow for the adjustment of the frequency division ratio and to allow for fine adjustment of the frequency division ratio as taught by Berquist. Addtionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the frequency divider 16 of Hsieh with that of Berquist because as the Hsieh reference is silent on the exact structure of the frequency divider one of ordinary skill in the art would have been motivated to use any art-recognized equivalent frequency divider including one that allows for fractional and external control as the one taught by Berquist.

Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh 6,737,927 (Hsieh) in view of Segawa et al. 6,342,818 (Segawa) and in further view of Berquist et al. 6,542,044 (Berquist) as applied to claims 1, 5-15, 20, 21, 24-26, 28 and 29 above, and further in view of Vandegraaf 4,347,484 (Vandegraaf) of record.

The combination made obvious above utilizes single frequency divider arrangement 16 in Hsieh and 155 and 158 in Berquist. However, as disclosed by Vandegraaf an art recognized equivalent frequency divider is a frequency divider that is composed of a plurality of frequency dividers connected in series or cascade. Note Figure 10 of Vandegraaf. Therefore, because these two frequency divider arrangements means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a frequency divider arrangement composed of a plurality of series connected frequency dividers for the frequency divider of the invention made obvious above. The selection of any of these known equivalents to provide a frequency division function would be within the level of ordinary skill in the art.

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh 6,737,927 (Hsieh) in view of Segawa et al. 6,342,818 (Segawa) as applied to claims 1, 5-12,14, 20, 26 and 28 above, and further in view of Vandegraaf 4,347,484 (Vandegraaf) of record.

Hsieh and Segawa shows the use of a single frequency divider circuit 16 in Hsieh. However, as disclosed by Vandegraaf an art recognized equivalent frequency divider is a frequency divider that is composed of a plurality of frequency dividers connected in series or cascade. Note Figure 10 of Vandegraaf. Therefore, because these two frequency divider arrangements means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a frequency divider arrangement composed of a plurality of series connected frequency dividers for the frequency divider of the invention made obvious above. The selection of any of these known equivalents to provide a frequency division function would be within the level of ordinary skill in the art.

Claims 30-34, 36-41 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berquist et al. 6,542,044 (Berquist) in view of Van Amesfoort 5,712,596 (Van Amesfoort) and Segawa et al. 6,342,818 (Segawa).

Figure 2 and the relevant text of Berquist discloses a signal generator having a voltage controlled oscillation circuit (vco) 154, a control voltage input terminal formed by the intput terminal of the vco, a frequency divider 155, 158 that is for frequency dividing the output of the vco signal and a buffer amplifier 156 that is formed between the vco 154 and the frequency divider 155, 158. The buffer amplifier of Berquist clearly couples the oscillation signal output of the vco to the input of the frequency divider circuit as is clearly illustrated by Berquist. The output terminal of the frequency divider is a terminal although it is an internal terminal. Note that this is giving the broadest reasonable interpretation to the claims (See MPEP 2111). Also note that the frequency divider of Berquist is a fractional divider

(See column 4, around line 52). Also note that an adjustable fraction divider like that of Berquist provides for whole numbers (Note claim 40). Also note that the claims do not limit the frequency divider to be limited only to whole numbers.

Berquist is silent on the structure of the buffer amplifier 156.

One common art recognized equivalent form of buffer that is formed on the output of a vco is a common emitter amplifier buffer (Note "BUF" in Van Amesfoort).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the buffer 156 of Berquist with a common emitter amplifier buffer because as the Berquist reference is silent on the exact structure of the buffer amplifier structure one of ordinary skill in the art would have been motivated to use any art-recognized equivalent buffer amplifier structure including a common emitter buffer amplifier structure such as the one taught by Van Amesfoort.

Berquist is silent on the loop integrator being an external structure thereby providing an external signal to the input of the vco. However, it is common knowledge in the art that forming the filter element outside, i.e. external the integrated circuit or inside, i.e. internal the integrated circuit that includes a vco and a frequency divider are art recognized equivalent structures. See column 17 around line 60 of Segawa. Therefore, because these two filter means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute an external filter for an internal filter and a internal filter for a external filter in a vco based circuit such as that of Hsich. Thus when the external filter is utilized in Hsich this provides an external control voltage to the vco of Hsich.

With respect to claims like claim 32, Berquist is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that has the frequency control controlled by a FET functioning as a voltage controlled variable capacitor. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Berquist with one at employs a FET functioning as a voltage controlled variable capacitor because as the Berquist reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that has a FET functioning as a voltage controlled variable capacitor used to control the frequency of the vco.

With respect to claims like claim 32, Berquist is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that is formed utilizing CMOS technology. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Berquist with one that is formed utilizing CMOS technology because as

the Berquist reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that is formed utilizing CMOS technology.

With respect to claims like claims 37 and 38, Hsieh is silent on the construction of the vco. However, one conventional art recognized equivalent form of vco is one that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the vco of Hsieh with one that that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor wherein the frequency of oscillation of the vco is controlled by the external voltage applied to the varactor diode as the Hsieh reference is silent on the exact structure of the vco one of ordinary skill in the art would have been motivated to use any art-recognized equivalent vco including one that includes a varactor diode in a resonant circuit coupled to a base of an oscillating transistor wherein the frequency of oscillation of the vco is controlled by the external voltage applied to the varactor diode.

With respect to claims like claim 36, the combination made obvious above is silent on placing the ic on a circuit board with the control voltage terminal and the frequency division signal output terminals are provided on the end faces or on the underside of the circuit board. It is well-known to place ic's on circuit boards and provide the contacts on the underside of the circuit board so as to provide for a package that allows the mounting of the ic and the connection of the ic to other circuits. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the ic made obvious above on a circuit board with underside contacts so as to allow for the ic to be mounted and connected with other circuits in a device or system as is conventionally known in the art to do so.

Claims 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berquist et al. 6,542,044 (Berquist) in view of Van Amesfoort 5,712,596 (Van Amesfoort) and Segawa et al. 6,342,818 (Segawa) as applied to claims 30-33, 36-41 and 46 above, and further in view of Vandegraaf 4,347,484 (Vandegraaf) of record.

Berquist shows the use of a single frequency divider circuit 155 and 158. However, as disclosed by Vandegraaf an art recognized equivalent frequency divider is a frequency divider that is composed of a plurality of frequency dividers connected in series or cascade. Note Figure 10 of Vandegraaf. Therefore, because these two frequency divider arrangements means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a frequency divider arrangement composed of a plurality of series connected frequency dividers for the frequency divider of the invention made obvious above. The selection of any of these known equivalents to provide

a frequency division function would be within the level of ordinary skill in the art. Note that the use of a Digital to analog converter would be required to provide the control signal to the plurality of frequency dividers in the combination made obvious above but this necessary coupling means would be well within the skill of one of ordinary skill in the art.

Claims 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berquist et al. 6,542,044 (Berquist) in view of Van Amesfoort 5,712,596 (Van Amesfoort) and Segawa et al. 6,342,818 (Segawa) as applied to claims 30-33, 36-41 and 46 above, and further in view of Hsieh 6,737,927 (Hsieh).

The combination made obvious above and in particular Berquist is silent on the construction of the vco 154 and the buffer 156. In particular Berquist is silent on the vco having a balanced output and the buffer converting the balanced output to a unbalanced output.

Hsieh in Figure 1(a) discloses that the one art recognized equivalent form of vco and buffer arrangement for a phase locked loop is that of a vco that outputs a balanced signal and a buffer that converts the balanced signal to a unbalanced signal. Therefore, because these two vco with buffer means were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a vco that outputs a balanced signal with a buffer that then converts the balanced signal to a single ended signal for the vco and buffer of Berquist. The selection of any of these known equivalents to provide a variable frequency signal would be within the level of ordinary skill in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
01-01-2006

Michael B Shingleton
Primary Examiner
Group Art Unit 2817